REMARKS

Claims 18-26 are pending in the present application with claims 1-17 canceled in a preliminary amendment. Applicants note with appreciation the allowance of claims 18, 19 and 21-24. With entry of this Amendment, Applicants amend claims 20, 25 and 26 and add new claims 27-32. Reexamination and reconsideration are respectfully requested.

The Examiner rejected claims 20, 25 and 26 under 35 U.S.C. § 102(b) as being anticipated by Hanazawa et al. (US 5590364). The rejection is respectfully traversed.

The present invention relates to a tone signal apparatus suitable for saving power consumption. A digital signal processor in the tone signal apparatus executes signal processing based on instructions from microprogram steps. Power consumption is saved by stopping the supply of an operating clock signal to the digital signal processor during a part of one sampling period for inactive steps.

The present invention further allows a user to change the number of steps to be processed by the digital signal processor. A power saving screen (see Fig. 5) allows a user to input the number of permitted steps 33. Fig. 6 illustrates a flowchart resulting from the user's selection. Depending on the currently chosen effects, the control data of the digital signal processor is set accordingly (SP20) or the user is notified that an insufficient number of steps has been inputted in view of the chosen effects (SP14). The user has the choice of canceling the inputted number of steps or having the effects damped out.

Method claim 25 recites the steps of "generating control data indicative of a part of the steps not valid or effective in the set programs" and "stopping a supply of the operating clock to the signal processor in a given duration corresponding to the part of the steps of the set programs indicated by the control data" and has been amended to add steps directed to the inputting of a permitted number of steps.

In contrast, Hanazawa does not disclose the generating and stopping steps set forth above. Hanazawa is directed to an apparatus that allows a program in a digital signal processor to be

rewritten. The Examiner has noted that Col. 4, lines 26-54 discloses a mode selector 27 that synchronizes a STOP signal from the CPU 11 with a sampling clock signal. However, this does not disclose stopping the supply of the operating clock signal to the digital signal processor during a part of one sampling period for inactive steps. Nor does Hanazawa disclose the recited steps of claim 25 relating to inputting a permitted number of steps. Accordingly, Applicants respectfully submit that claim 25 is not anticipated by Hanazawa.

Applicants respectfully submit that claims 20 and 26 are not anticipated by Hanazawa for the reasons set forth above with respect to claim 25.

New method claim 28 recites the steps of "generating control data indicative of a part of the steps not valid or effective in one sampling period" and "stopping a supply of the operating clock to the signal processor in a given duration corresponding to the part of the steps of the set programs indicated by the control data" and, thus, is not anticipated by Hanazawa as discussed above. Furthermore, claim 28 further includes steps of inputting a permitted number of steps, detecting a number of free steps not used by the signal processor, listing a menu of programs which can be selected within the detected number of free steps and selecting a program. Hanazawa does not disclose any such steps. Accordingly, Applicants respectfully submit that that claim 28 is not anticipated by Hanazawa for this reason as well.

Applicants respectfully submit that claims 27 and 29 are not anticipated by Hanazawa for the reasons set forth above with respect to claim 28.

New method claim 31 recites detecting an inactive range of steps in the number of the steps executed by the signal processor, writing clock-off and clock-on instructions according to the detected number of steps, "generating control data indicative of a part of steps not valid or effective and ranging from a step for executing the clock-off instruction to another step for executing the clock-on instruction in the set program" and "stopping a supply of the operating clock to the signal processor in a given duration corresponding to the part of the steps of the set program indicated by the control data." Hanazawa does not disclose detecting inactive steps and performing the

remaining recited steps. Accordingly, Applicants respectfully submit that that claim 30 is not anticipated by Hanazawa for this reason.

Applicants respectfully submit that claims 30 and 32 are not anticipated by Hanazawa for the reasons set forth above with respect to claim 31.
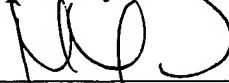
In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If, for any reason, the Examiner finds the application other than in condition for allowance, Applicants request that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5630 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 393032023101.

Dated: February 17, 2004   Respectfully submitted,

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